REMARKS/ARGUMENTS

The Office Action mailed June 11, 2003 has been reviewed and carefully considered. Claims 26-33 are canceled. Claims 1, 5, and 16 are amended. Claims 1-25 and 34 are pending in this application, with claims 1 and 16 being the only independent claims. Reconsideration of the above-identified application, as herein amended and in view of the following remarks, is respectfully requested.

In the Office Action mailed June 17, 2002, claims 4-11 and 16-25 are currently withdrawn from consideration. The Examiner has identified independent claim 1 as generic. Upon allowance of independent claim 1, dependent claims 4-11 and 16-25 are entitled to consideration.

Claims 1-3 and 13-15 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 6,049,250 (Kintis).

Claim 12 stands rejected under 35 U.S.C. §103 as unpatentable over Kintis in view of U.S. Patent No. 4,970,478.

The present invention relates to an attenuator comprising first and second transmission lines TL1 and TL2 connected in series between an input terminal IN and an output terminal OUT (see page 7, lines 3-4; Fig. 2). Three variable shunt elements having FETs are connected to ground. A first variable shunt element R1 has one end connected between the input terminal IN and the first transmission line TL1, a second variable shunt element R2 has one end connected between the first and second transmission lines TL1, TL2, and a third variable shunt element R3 has one end connected between the second transmission line TL2 and the output terminal OUT. The attenuation of the signal in the attenuator is controlled by a control signal input to a gate terminal of the FET connected in each shunt element (see Fig. 3).

Independent claim 1 has been amended for clarification to change the term serially to --in series--. Independent claim 1 now recites "a first transmission line connected in series between said input terminal and said output terminal and having a first transmission line impedance", "a first variable shunt element having one leg connected at a point between said first transmission line and said input terminal, said first variable shunt element having a variable impedance", "a second variable shunt element having one leg connected at a point between said first transmission line and said output terminal, said second variable shunt element having a variable impedance", and "a control signal terminal connected to each of said first and second variable shunt elements so that an attenuation level of said first attenuation circuit is controllable by a control signal input to said control signal terminal".

Kintis discloses a distributed feedback distributed amplifier 60 with a plurality of amplifier stages 62, 64, 66 (col. 3, lines 42-44). Each amplifier stage includes an FET 68, 70, 72 configured in a common source configuration (col. 3, lines 45-46). The gate terminals of the FETs 68, 70, 72 are connected to a common gate line 74 (col. 3, lines 49-51). The drain terminals of the FETs 68, 70, and 72 are connected to a common drain line 76 (col. 3, lines 51-53). Input signals are applied to the gate line 74 and output signals are output from terminals 80 connected to the drain line 76 (col. 3, lines 63-66). The FETs are biased by a gate bias voltage V_{GG} and a drain bias voltage V_{DD} (col. 4, lines 13-26). The gain of the amplifier 60 is controlled by varying the values of feedback resistors 100, 102, 104 and source resistors 94, 96, 98 (col. 4, lines 60-62).

According to Kintis, the common gate line 74 includes a plurality of microstrip lines serially connected between the input terminal and ground and the common drain line 76 includes a plurality of microstrips serially connected between the output terminal and ground. The common gate line 74 and the common drain line 76 are connected by a plurality of parallel amplifier stages.

Accordingly, neither the common gate line nor the common drain line is connected serially between the input and output terminals. More specifically, the Examiner states that microstrip 63 is considered the first transmission line of the claimed invention. However, microstrip 63 is not connected in series between the input and output terminal. Rather, microstrip is connected to the output terminal in parallel with the amplifier stage 62. Accordingly, Kintis fails to disclose a first transmission line connected in series between the input terminal and the output terminal, as recited in independent claim 1.

Furthermore, the Examiner states that the bias voltage V_{DD} is a control signal for controlling the attenuation. However, it is respectfully submitted that the bias voltage V_{DD} is merely a voltage applied to place the transistor in a proper operating range (see col. 4, lines 13-21). Kintis specifically discloses that the gain, i.e., attenuation, is varied by varying the values of feedback resistors 100, 102, 104 and source resistors 94, 96, 98 (col. 4, lines 60-62). Accordingly, Kintis fails to show the "a control signal terminal connected to each of said first and second variable shunt elements so that an attenuation level of said first attenuation circuit is controllable by a control signal input to said control signal terminal", as recited in independent claim 1.

For all of the above reasons, independent claim 1 is <u>not</u> anticipated by Kintis under 35 U.S.C. §102.

Independent claim 1 is also allowable over Kintis under 35 U.S.C. §103. The present invention relates to an attenuator in which the signal passes through the transmission line in series from an input to an output and is attenuated by shunt elements as required to achieve the desired attenuation. Kintis relates to an amplifier in which an input signal is connected to a gate terminal of each independent amplifier stage and an output is connected to a drain terminal of each independent amplifier stage. Accordingly, there is no teaching or suggestion in Kintis for the

claimed configuration in which the transmission line is arranged in series between the input and output terminals. Therefore, independent claim 1 is also allowable over Kintis under 35 U.S.C. §103.

Dependent claims 2-15 and 34, being dependent on independent claim 1, are allowable for at least the same reasons as is independent claim 1.

New claim 34 further recites that the control signal is input to a gate terminal of the transistor in the shunt elements. Support for this limitation is found on page 8, lines 20-21, in the specification. In contrast, Kintis discloses that the gate terminal of the transistor is connected to the input terminal by the gate line 74. Therefore Kintis does not disclose a control signal connected to the gate terminal. Claim 34 is allowable for this additional reason.

The application is now deemed to be in condition for allowance and notice to that effect is solicited.

Respectfully submitted,

COHEN, PONTANI, LIEBERMAN & PAVANE

By 

Alfred W. Froebrich
Reg. No. 38,887
551 Fifth Avenue, Suite 1210
New York, New York 10176
(212) 687-2770

Dated: October 10, 2003